REMARKS

Claims 1 - 41 were pending in the present application for patent as of the Office Action of June 10, 2004. In the Office Action of June 10, 2004, the Examiner objected to claims 29 and 30 as being dependent on the wrong claims, rejected claims 26 and 28 under 35 U.S.C. 102(e) as being anticipated by U.S. Publication Number 2004/0041189, Voshell et al., rejected claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. in view of U.S. Patent Number 6,649,476, Forbes and U.S. Publication Number 2001/0024858, Schulz et al., rejected claims 13 and 21 under 35 U.S.C. 103(a) in view of Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of U. S. Publication Number 2004/0041188, Bissey, rejected claim 16 under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. in view of Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of U.S. Patent Number 6,511,884, Quek et al., rejected claim 27 under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. as applied to claims 26 and 28 and further in view of Bissey, and rejected claims 29 and 30 under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. as applied to claims 27 and 28 and further in view of Forbes et al.

Because of a previous restriction requirement, claims 31 - 41 were withdrawn from consideration. In an effort to advance the application to a final disposition, the applicants have canceled the withdrawn claims 31 - 41.

Claims 29 and 30 were objected to as being dependent on the wrong claims. In response, the applicants have amended claims 29 and 30 to depend upon claim 26 instead of claim 24.

Claims 26 and 28 were rejected under 35 U.S.C. 102(e) as being anticipated by Voshell et al. Voshell et al. discloses a vertically oriented access transistor for a memory. The applicants believe that Voshell et al. does not show or suggest a method of forming a semiconductor structure as claimed in amended claim 26. For example, Voshell et al. does not show or suggest "removing the layer of gate material over the semiconductor fin to leave a first gate along the first sidewall and a second gate along the second sidewall". In Voshell et al. the gate material is formed around the pillar but is not formed over the top and then removed as claimed in claim 26. Also, Voshell et al. does not show or suggest forming symmetrical

source and drain regions as claimed in amended claim 26. In Voshell et al., the source and drain regions are not symmetrical because one doped region is formed in the top of the pillar and the other doped region is formed in the semiconductor material at the other end. Therefore, Voshell et al. does not solve the same problem or offer the same advantages as the semiconductor structure claimed in amended claim 26. For example, in the present invention, the gate length can be changed without a process change simply by changing the length of the gate material ("L" in FIG. 24). This does not appear to be possible in Voshell et al.

Regarding the rejection of claim 28, the applicants believe that the above comments regarding the rejection of amended claim 26 apply. Also, the applicants believe that Voshell et al. does not show or suggest the method of claim 28, where the first gate comprises a first plurality of gate portions electrically connected together. The examiner referred to FIG. 1 of Voshell et al. to show gate portions electrically connected together. However, FIG. 1 of Voshell et al. shows a plurality of gates connected together via a word line. Voshell et al. does not show or suggest portions of the same gate electrically connected together as claimed in claim 28. Therefore, the applicants believe that claims 26 and 28 are allowable over Voshell et al.

Claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. in view of Forbes and Schulz et al. The applicants have amended claims 1 and 17. Voshell et al. in view of Forbes and Schulz et al. does not show or suggest the present invention as claimed in amended claims 1 and 17. Generally, Forbes discloses a logic array having a plurality of vertical transistors. The vertical transistors of Forbes only have one gate (see column 7, lines 26 - 30). Schulz et al. also discloses a vertical transistor, but the source and drain regions are not symmetrical and the gate electrodes are coupled together to receive the same signal. Also, gate material is not etched from the top of the semiconductor structure as claimed in amended claim 1. Therefore, combining Voshell et al., Forbes, and Schulz et al. does not result in the present invention as claimed in amended claim 1. In addition, Applicants believe that the comments above regarding the rejection of claims 26 and 28 also apply to the rejection of claim 1.

Regarding the rejection of claims 2 - 12, 14 - 15, 18 - 20, and 22 - 25, the applicants believe that the comments above concerning the rejection of claims 1, 17, 26, and 28 also

apply to the rejection of claims 2 - 12, 14 - 15, 18 - 20, and 22 - 25, and that claims 2 - 12, 14 - 15, 18 - 20, and 22 - 25 are allowable over Voshell et al. in view of Forbes and Schulz et al.

Claims 13 and 21 were rejected under 35 U.S.C. 103(a) in view of Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of Bissey. The comments above concerning claims 1 and 17 also apply to the rejection of claims 13 and 21, and the claims 13 and 21 are allowable over Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of Bissey et al. Bissey et al. discloses a vertical pillar structure similar to the pillar structure disclosed in Voshell, except Bissey et al. discloses two gates (FIG. 20) on the vertical pillar structure and a logic circuit. However, Bissey et al. does not show or suggest a method as claimed, where the source and drain regions are symmetrical. Also, Bissey et al. does not show or suggest etching through the layer of gate material on the top surface. In Bissey et al. the gate material is formed around the pillar but is not formed over the top and then etched as claimed Also, Bissey et al. does not show or suggest forming symmetrical source and drain regions as claimed. In Bissey et al., the source and drain regions are not symmetrical because one doped region is formed in the top of the pillar and the other doped region is formed in the semiconductor material at the other end. Therefore, Bissey et al. does not solve the same problem or offer the same advantages as the present invention. For example, in the present invention, as claimed, the gate length can be changed without a process change simply by changing the length L (shown in FIG. 24) of the gate material. This does not appear to be possible in Bissey et al.

Claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. in view of Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of Quek et al. The comments above also apply to the rejection of claim 16. In addition, the gates of Quek et al. are formed like side wall spacers and are referred to as "spacer gates". Therefore, the applicants believe that claim 16 is allowable over Voshell et al. in view of Forbes and Schulz et al. as applied to claims 1 - 12, 14 - 15, 17 - 20, and 22 - 25 and further in view of Quek et al.

Claim 27 was rejected under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. as applied to claims 26 and 28 and further in view of Bissey. Claims 29 and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. as applied to claims 27 and 28 and further in view of Forbes et al. The applicants believe that the comments above

regarding the rejection of claims 26 and 28 also apply to the rejection of claims 27, 29, and 30, and that claims 27, 29, and 30 are allowable over the cited references.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed June 10, 2004, the applicants respectfully request the reconsideration and allowance of claims 1 - 30; thereby placing the application in condition for allowance.

Respectfully submitted,

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